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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,543	08/04/2000	Rajendra K. Talluri	TI-28919	1760
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EXAMINER NGUYEN, LUONG TRUNG				
ART UNIT 2622		PAPER NUMBER		
NOTIFICATION DATE 10/02/2008		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary

Application No.

09/632,543

Applicant(s)

TALLURI ET AL.

Examiner

LUONG T. NGUYEN

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 September 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
- Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 9/17/2008 has been entered.

Response to Arguments

2. Applicant's arguments filed on 9/17/2008 have been fully considered but they are not persuasive.

In re page 5, Applicants argue that Duncan does not teach or recite an integrated circuit that utilizes parameter-driven address generation and looping control.

In response, regarding claim 1, the Applicants amended claim 1 with limitation "wherein the integrated circuit that utilizes parameter-driven address generation and looping control." The Examiner considers that Duncan et al. does disclose this limitation. Duncan discloses the digital camera in figures 1-2 utilizes address bus, data bus, control signal bus in figure 4 corresponds to

parameter-driven address generation for controlling image transform processor 206 as in looping control shown in figure 2.

In re pages 5-6, Applicants argue that Safai and Mizutani do not suggest or show a motivation for modifying the reference or to combine the reference teachings.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, regarding claim 3, Safai fails to specifically disclose an image compression unit separate from said second processor, said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory. However, Mizutani et al. discloses a digital still camera 1 includes compression/expansion circuit 29, which is separated from memory controller 22, compresses image data to store in image memory 32, and expands the compressed image data (figures 2-3, column 6, lines 25-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Safai by the teaching of Mizutani et al. in order to compress image data before storing image data into a memory. This increases the amount of image data to be stored in the memory.

Claim Objections

3. Claim 6 is objected to because of the following informalities:

Claim 6 (line 2), “including IfSA” should be changed to --including IrDA--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Duncan et al. (US 6,597,394).

Regarding claim 1, Duncan et al. discloses an integrated circuit for a digital still camera, for performing image pipeline tasks, comprising:

a first programmable processor programmed (microprocessor 202, figure 2, column 4, lines 1-33) to run control functions, said first processor coupled to a user interface (display 210, figure 2), a controller for memory (controller for memory 203, figure 2, column 1, lines 1-33), and a controller for image acquisition (image sensor 106, figure 2);

a second programmable processor (programmable addressing block 410 included in image transform processor 206 which performs compression operation, figures 2, 4, column 5, line 60 – column 6, line 31) programmed to run image processing and compression functions,

said second processor coupled to said first processor (figure 2 shows that image transform processor 206 coupled to microprocessor 202);

a third processor coupled (arithmetic block 450, figure 4) to said second processor (programmable addressing block 410, figure 2), said third processor including more than one parallel multiply and accumulate units (arithmetic block 450 includes four multipliers 630-633 which is coupled to latches 640-643, figure 6A, column 15, lines 15-62), wherein the integrated circuit that utilizes parameter-driven address generation and looping control (Duncan discloses the digital camera in figures 1-2 utilizes address bus, data bus, control signal bus in figure 4 corresponds to parameter-driven address generation for controlling image transform processor 206 as in looping control shown in figure 2).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Safai (U S 6,642,956) in view of Mizutani et al. (U S 6,674,464).

Regarding claim 3, Safai discloses an integrated circuit for a digital still camera, comprising a first programmable processor programmed (microprocessor 312, figure 3, column 7, lines 7-28) to run control functions, said first processor coupled to a user interface (display 318 and touch screen 319, figure 1), a controller for memory (display controller 317, figure 1),

and a controller for image acquisition (image capture unit 302); and a second programmable processor (digital image processor 310, figure 3, column 5, lines 45-58) programmed to run image processing (performing some processing of digital images, column 5, lines 50-54) and compression functions (digital compressor 426, figure 4, column 9, lines 43-55), said second processor coupled to said first processor (figure 3 shows that digital image processor 310 coupled to microprocessor 312), wherein the integrated circuit that utilizes parameter-driven address generation and looping control (Safai discloses the microprocessor 312 of digital camera 300 is capable of directing the retrieval of digital images stored in memory 314 or local memory 311, figure 3, column 7, lines 7-45. This indicates that the digital camera 300, as shown in figure 3, utilizes parameter-driven address generation and looping control).

Safai fails to specifically disclose an image compression unit separate from said second processor, said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory. However, Mizutani et al. discloses a digital still camera 1 includes compression/expansion circuit 29, which is separated from memory controller 22, compresses image data to store in image memory 32, and expands the compressed image data (figures 2-3, column 6, lines 25-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Safai by the teaching of Mizutani et al. in order to compress image data before storing image data into a memory. This increases the amount of image data to be stored in the memory.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (US Re. 36,338) in view of Hsieh et al. (US 5,969,750).

Regarding claim 4, Fukuoka discloses an integrated circuit for a digital still camera, comprising a first programmable processor programmed (CPU 11, figure 1, column 4, lines 17-39) to run control functions, said first processor coupled to a user interface (display section 19 and operating section 20, figure 1, column 4, lines 57-62), a controller for memory (CPU 11, figure 1, column 4, lines 36-39), and a controller for image acquisition (CPU 11, figure 1, column 4, lines 35-39); a digital image processing unit (digital signal processing 6, figure 1) separate from said first and second processors, said image processing unit arranged for real-time image sequence (video) processing, said image processing unit controlled in real-time by said first processor, wherein the integrated circuit that utilizes parameter-driven address generation and looping control (Fukuoka discloses the construction of a file of image data and sound recorded to the memory card 10, which includes an odd JPEG file, an even JPEG file, a sound file, figure 2, column 5, lines 10-24; and regenerating a still image, figure 3m column 5, lines 23-56. This indicates that the electronic still camera, as shown in figure 1, utilizes parameter-driven address generation and looping control).

Fukuoka discloses compress and extending image data 7 is coupled to CPU 11 (figure 1m column 4, lines 30-39). Fukuoka does not disclose compress and extending image data 7 is a second programmable processor programmed to run image processing and compression functions. However, Hsieh et al. discloses camera 110, which comprises bit rate reduction circuit 115, which is a programmable compressor (figure 5, column 6, lines 27-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

modify the device in Fukuoka by the teaching of Hsieh et al. in order to provide a camera, in which compression rate can be changeable.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 6,597,394) in view of Fukuoka (U S Re. 36,338).

Regarding claim 5, Duncan et al. fails to specifically disclose an audio input coupled to said second processor, said second processor programmed to decode audio and said first processor programmed to output said decoded audio. However, Fukuoka discloses an electric still camera includes microphone 12 for inputting sound, microphone 12 is coupled to the sound data compressing-extending circuit 15 (second processor). The sound data are extended by the sound data compressing-extending circuit 15, and outputted as an audio signal through D/A 22 and amplifier 23 by the control of central processing 11 (first processor), figure 1, column 5, lines 4-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Duncan et al. by the teaching of Fukuoka in order to record sound data together with image data.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 6,597,394) in view of Safai (US 6,642,956) further in view of Mizutani et al. (US 6,674,464).

Regarding claim 6, Duncan fails to specifically disclose camera peripherals including USB, and compact flash/smart media interface.

However, Safai discloses a digital camera, which comprises camera peripherals including USB, and compact flash/smart media interface (USB port, PCMCIA port, figure 3, column 7,

lines 13-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Duncan et al. by the teaching of Safai in order to use only one cable (USB) to transmit data and power. This reduces cost of the device.

Duncan et al. and Safai fail to specifically disclose camera peripherals including IrDA, NTSC/PAL encoder. However, Mizutani et al. discloses a digital still camera 1 includes an NTSC/PAL encoder 23, and IrDA interface 45 (figure 2, column 5, lines 39-40, column 6, lines 53-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Duncan et al. and Safai by the teaching of Mizutani et al. in order to display image data on a TV monitor.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LTN
9/28/08

/LUONG T NGUYEN/
Examiner, Art Unit 2622